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A Built-in Self-Test System for External DRAM

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Abstract

In the fast-growing Integrated Circuits (IC) industry, memory is one of the few keys to have systems with improved and fast performance. Only one transistor and a capacitor are required for Dynamic Random-Access Memory (DRAM) bit. It is widely used for mass storage. Although the high-efficiency tests are performed to provide the reliability of the memories, maintaining acceptable yield and quality is still the most critical task. To perform a high-speed effective test of DRAM memories, a built-in self-test (BIST) mechanism is proposed.

Keywords: Built-in Self-Test System, external DRAM memory, DRAM memory faults, System on Chip.

1. Introduction

One of the important and critical requirements for a System on Chips (SoCs) is the reliability of memories. As memories are used in more and more complex designs, the occurrence probability of manufacturing defects becomes very high. And, testing of embedded memories is a real challenge. Depending on the availability of voltage sources, memories are divided into two categories: volatile memories, which require connection to the power source to keep in the stored data, and non-volatile memories, which can keep the data without a power supply connection. The volatile and non-volatile memories have different structures and functions. Therefore, they have different testing methodologies. The popular type of volatile memory is Random-Access Memory (RAM) [1].

Dynamic Random-Access Memory (DRAM) is one of the most well-known memory components in the industry, primarily used as the main memory in personal computers (PCs), workstations, and mainframes. The amount of DRAM devices found in a PC has a significant impact on its general performance and is considered an important parameter in PC specifications. DRAMs are usually produced in the form of an integrated circuit chip, which might be packaged in many ways, depending on the specific application and the performance of the DRAM. DRAMs are also used in wireless mobile devices, such as smartphones, tablets, etc. [2].

2. DRAM Memory Overview

2.1. DRAM memory structure

Unlike SRAM cells, which store data on the output of the standard cell, DRAM cells store information on a capacitor in the form of charge. This charge leaks off over time, causing data loss. To stop this process, DRAM cells must be periodically refreshed. Fig. 1-b shows the DRAM memory bit.

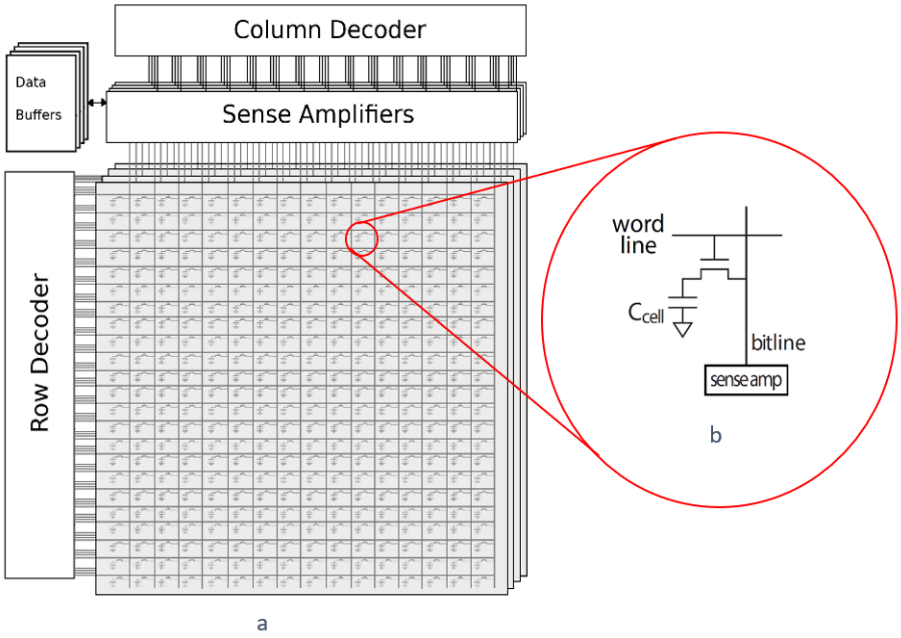

Fig. 1. a) DRAM memory simple array example, b) A bit-cell of DRAM [3].

A 1-transistor DRAM cell contains one transistor and one single capacitor. The data is stored on a capacitor as a charge, to which the transistor will give access. When performing the write operation (by enabling the corresponding word line), the state that the capacitor should take on is in word lines. The word line is opened, so the sense amplifier is forced to the corresponding voltage state. When reading, the capacitor shares its charge with the bit line, causing a voltage change on it.

The charge stored on each capacitor is simply too small to be read directly and is instead measured by a circuit called a sense amplifier. The charge is set by the sense amplifier. The sense amplifier, which is connected to the bit line, detects the voltage change, and amplifies it. After that, the voltage can be interpreted as a logical 0 or 1 by an external driver. However, due to the transistors leakage on the cut-off state, the stored charge is gradually lost, thus the necessity for periodical refresh operation to stop the data corruption. In Figure 1-a DRAM memory array sample is presented. The grey section is the memory array designed as a grid of rows and columns. A group of decoders provides access of rows and columns, selecting one intersection within the memory array. The logical representation of a physical defect is named a fault (the line is broken, short between lines, etc.) in the memory. Depending on the SoC manufacturer, the set of faults in memory may vary [3].

2.2. DRAM Memory Fault Detection Mechanisms

The increase of memory components in IC and the increase of memory complexity makes memory testing and fault analysis significantly important. DRAM memory testing mechanisms can be divided into 2 groups: the retention testing and functional testing. Retention testing mechanism shows the leakage currents by performing read and write operations containing a special delay between each other. In the case of functional testing, March element is a sequence of read and write operations, which are applied to the memory cells consecutively to detect not only cell defects but also cell-to-cell bridge and coupling faults [4]. There are several requirements to have a successful test mechanism.

Fault detection: This step is the basic requirement for testing. The test mechanism must report a fail after March element execution on memory that contains fail.

Fault localization: The test mechanism should be able to localize faulty memory cell or group of cells.

Fault diagnosis: The test mechanism should be able to indicate the exact physical root cause behind the detected fault.

2.3. DRAM Memory Faults

2.3.1. Common faults for memories

The most common faults are classified into two groups shown below in Fig. 2.

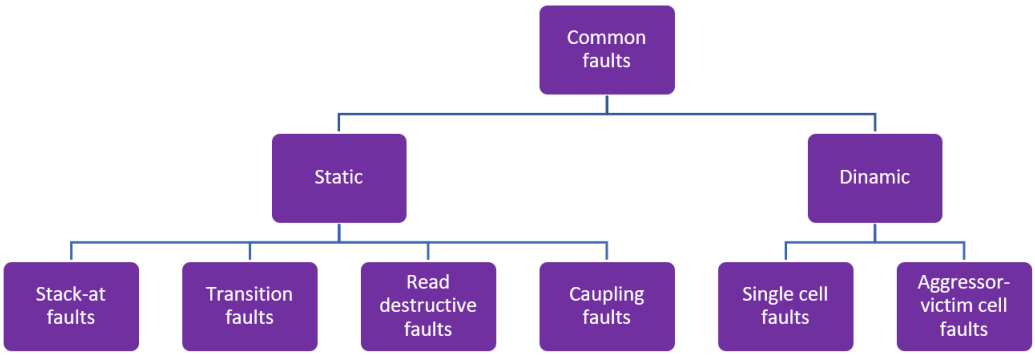

Fig. 2. Common faults of the memories.

Static faults: To detect static faults, an execution of the single operation is needed. The common static fault is Stuck-at fault, when the cell is stuck at static value (ST0 Stuck at 0, ST1 Stuck at 1) and write operations do not make any changes on it. Static fault group contains also Transition faults (i. e., Wired-AND, Wired-OR, etc.), read destructive faults, coupling faults, etc.

Dynamic faults: To detect dynamic faults, an execution of at least two consecutive operations are needed. For example, the cell value can be flipped, when two consecutive read operations are applied to that cell (single-cell dynamic fault). On the other hand, two consecutive write operations applied to a cell (aggressor cell) can change the value of the neighbor cell (victim cell). Because of manufacturing complexity, a single march test algorithm covering all static and dynamic faults may be unacceptable for all the manufacturers.

So, there are many march test algorithms proposed for complexities, different types of faults, and their coverages [1].

2.3.2. DRAM Memory Specific Physical Faults

Figure 3 shows a simple DRAM memory cell and the relation between faults and physical defects.

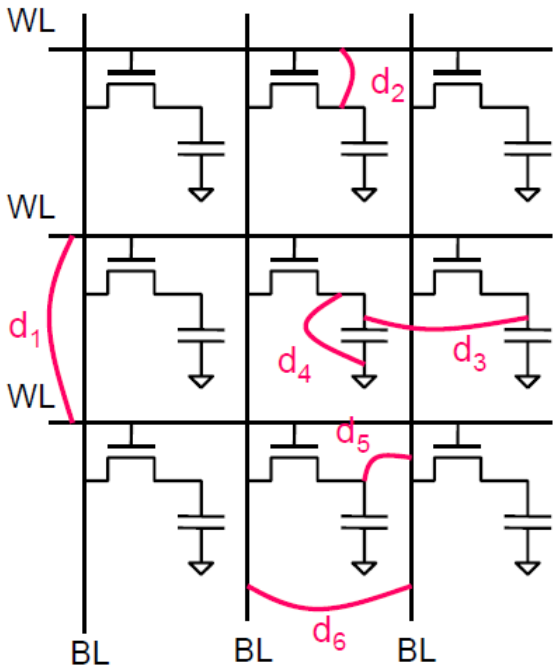

Fig. 3. A simple DRAM memory cell and physical defects [5].

A short between two WLs, shown as a defect d1, causes bridging AND fault between pairs of cells located in the same column for the two shorted WLs.

A short between capacitor and WL, presented as a defect d2, causes WL SA1 fault.

A short between two neighbor capacitors, presented as a defect d3, causes a state coupling fault.

A short between a capacitor and the ground, presented as a defect d4, causes bits SA0 fault.

A short between capacitor and BL, presented as a defect d5, is a bridging AND fault with all cells in the same column.

A short between two neighboring BLs, presented as a defect d6, is a bridging AND fault between pairs of cells on the same word line and on the shorted bit lines [5].

2.3.3. DRAM Memory Specific Voltage and Timing Faults

This kind of DRAM fault has two main causes. A: voltage-dependent faults, because of improperly set of voltages, B: time-dependent faults, because of capacitors leakage currents [4]. Fig. 4 presents the faults described above.

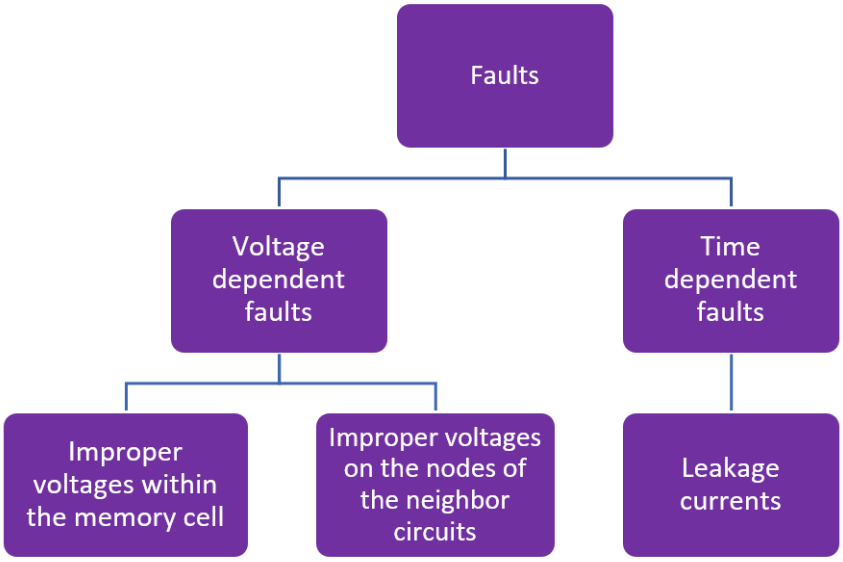

Fig. 4. DRAM memory specific voltage and timing faults.

3. The Overview of the Built-in Self-Test System for External Memories

3.1. Built-in Self-Test Systems General Structure

The BIST System is a complete RTL assembly intended for at-speed testing and diagnostic of external memories. The general structure of the BIST System is described below in Figure 5.

One of the components of the BIST System is Selection Logic. There are two input drivers for that selector. The first one is User Control Logic, which drives external memory and runs it in functional mode. In that case, the BIST System does not have an access to the memories. The second driver is Test Control Logic. In this case, the BIST System has access to the external memories, so it can run the memories functionality in test mode. The User Control Logic also can have a direct access to PHY, but BIST System will have an access only with selection signal activation.

The select signal of the multiplexer will be driven by the BIST System. Obviously, when the memories are in functional mode, the select signal will be 0, otherwise 1 (memories are in test mode).

Logically, the first iteration is to run the external memory in test mode. The Test Control Logic will drive multiplexers input, run Built-in Self-Test engine, confirm that the memory has no defects, then give the control to the User Control Logic. After that User Control logic will drive the multiplexer and run the external memory in functional mode.

3.2. Built-in Self-Test Systems Main Components

The Built-in Self-Test System has a lot of components, which are responsible for external memories testing and faults diagnostics. Some of those components are presented below in Table 1.

The components are working with each other with a hand shaking method. Once one

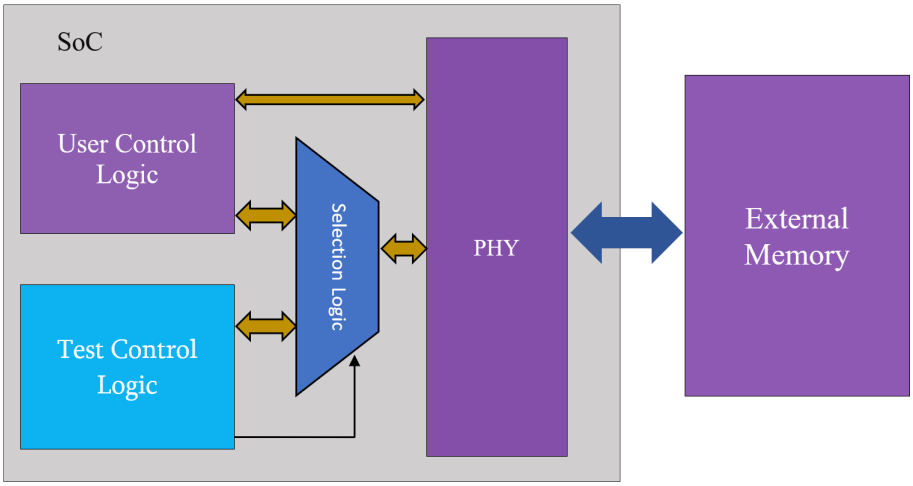

Fig. 5. A Built-in Self-Test Systems general structure.

component is generating some logic, the neighbor one is receiving that and starting to work. At that time the first one is waiting for response signal to do some analysis. The BIST System has also the diagnostic feature, which is able to identify the fault location of the external memories. After fault localization, User Logic Control can read that information from the Test Control Logic in some ways.

Table 1: BIST Systems main components

Address generator	Generates address based on memory configuration.
Data generator	Generates input data for the external memory, based on memory configuration.
BIST controller	Runs BIST mechanism for external memories, based on information from Address and Data generators.
Data comparator	Compares the output data of the external memories with expected data.

3.3. Built-in Self-Test Systems Features

The Built-in Self-Test System has a lot of features. The System has a lot of developed optimal test algorithms to decrease the risk of failure in the external memories [6, 7]. There are several types of algorithms. The default test algorithms are proposed for the detection of the most probable bunch of faults, that are common for different types of memories (hardwired ones). The second type of the algorithms is proposed for detection of the remaining types of the most known faults (full manufacturing algorithms). And the last type of the algorithms is proposed for specific types of faults, for specific cases or for user debug (programmable algorithms).

With those algorithms, different types of test operations can be executed (such as single cycle operations, etc.) to detect different types of faults. The algorithms are developed based on realistic faults of memories. The BIST System can run the test engine in some different ways, based on the memory configuration.

4. Conclusion

In this paper, different types of faults specific to external DRAM memories have been presented as well as the steps of fault detection mechanisms were described. The BIST System was developed for this purpose and its most important features were described. The System gives an opportunity to test external memories, detect faults, localize them, and report the corresponding fault information. In addition, the developed BIST System is capable of running various types of test algorithms, which are intended to detect different types of faults referred in the paper.

References

[1] S. Martirosyan and G. Harutyunyan, "An efficient fault detection and diagnosis methodology for volatile and non-volatile memories", *Proceedings of International Conference Computer Science and Information Technologies (CSIT)*, Yerevan, Armenia, pp. 1-3, 2019.

[2] Z. AL-ARS, *DRAM Fault Analysis and Test Generation*,Electrical Engineering, Mathematics and Computer Science, doctoral thesis, 2005.

[3] Stephen St. Michael, Introduction to DRAM (Dynamic Random-Access Memory), Online. Available: https://www.allaboutcircuits.com/technical-articles/introduction-to-dram-dynamic-random-access-memory, 2019.

[4] K. Manju Priya, M. Menaka, "A survey on dram testing and its algorithms", *International Journal of Computer Science Trends and Technology (IJCST)*, vol. 2, no. 5, pp 1-3, 2014.

[5] Jin-Fu Li, *Advanced Reliable Systems (ARES)*, Dept. of Electrical Engineering National Central University Jhongli, Taiwan.

[6] Y. Zorian, S. Shoukourian, K. Darbinyan, V. Vardanian and G. Harutyunyan, A Robust Solution for Embedded Memory Test and Repair, *IEEE Asian Test Symposium*, pp. 3-5, 2011.

[7] V. A. Vardanian, Y. Zorian, G. Harutunyan, Minimal March tests for detection of dynamic faults in random access memories, *Journal of Electronic Testing: Theory and Applications (JETTA)*, vol. 23, no. 1, pp. 1-3, February 2007.

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Ներկառուցված ինքնաթեստավորման համակարգ արտաքին դինամիկ հիշողությունների համար

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Ամփոփում

Արագ զարգացող ինտեգրալ սխեմաների արդյունաբերության մեջ հիշողությունը այն հիմնական տարրերից մեկն է, որը հնարավորություն է տալիս կատարելագործել համակարգը և մեծացնել համակարգի արագագործությունը: Մեկ բիթ դինամիկ հիշողությունը պահանջում է միայն մեկ տրանզիստոր և մեկ ունակություն: Այն լայնորեն օգտագործվում է մեծ ծավալի տվյալներ պահպանելու համար: Չնայած հիշողությունների հուսալիությունն ապահովելու համար կատարվում են բարձր արդյունավետությամբ թեստեր, ընդունելի պիտանի ելքի և որակի պահպանումը դեռևս ամենակարևոր խնդիրն է: Դինամիկ հիշողության արագագործ և արդյունավետ թեստավորում իրականացնելու համար առաջարկվում է ներկառուցված ինքնաթեստավորման համակարգ:

Բանալի բառեր՝ ներկառուցված ինքնաթեստավորման համակարգ, արտաքին դինամիկ հիշող սարք, դինամիկ հիշող սարքի անսարքություններ, համակարգ բյուրեղի վրա:

Архитектура встроенного самотестирования для динамических памятей

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Аннотация

В быстрорастущей индустрии интегральных схем, память - одна из немногих ключей к созданию систем с улучшенной и быстрой производительностью. Для бита динамической памяти с произвольным доступом требуются только один транзистор и один конденсатор. Она широко используется для хранения массовой информации. Несмотря на то, что для обеспечения надежности памятей выполняются тесты с высокой эффективностью, поддержание приемлемого подходящего выхода и качества по-прежнему является наиболее важной задачей. Для быстрого и эффективного тестирования динамической памяти предлагается встроенный механизм самотестирования.

Ключевые слова: встроенная система самотестирования, внешняя динамическая память, неисправности динамических устройств памяти, система на чипе.