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BIST Architecture for Magnetic Memories

Armen V. Babayan

National Polytechnic University of Armenia
e-mail: Armen.Babayan@synopsys.com

Abstract

Magnetic random-access memory (MRAM) is one of the emerging memory technologies, which can be considered as the next universal memory because of its good parameters. Nevertheless, this type of memory is not guaranteed from defects and it is very important to understand the fault typology and develop a test solution that addresses these faults. In this paper a Built-in Self-Test (BIST) solution is presented, which is specifically tailored for MRAMs and efficiently deals with MRAM specific faults.

Keywords: Memory BIST, Memory testing, Magnetic memory, Emerging memory, System on Chip.

1. Introduction

Innovative technologies require effective solutions to increase the reliability of systems in the industry of the integrated circuits (IC). Devices like memories are sensitive to external influences that can cause a system failure. Nowadays memories are the most commonly used devices in electronics. In recent decades, different types of memories have been invented, each of which had certain parametric and functional characteristics. Few examples of such memories can be found in the literature, as demonstrated below.

- Macro block, which consists of 0.021um^2 SRAM bit cells. Macro operates up to 2GHz at 0.95V. 5nm FinFET technology is used [1].
- 16Gb DRAM with speed 18Gb/s/pin and 1.35V VDD [2].
- 16Tb Flash memory is proposed in [3], which works with speed 1.8GB/s/pin. 20nm CMOS technology is used.

On the other hand, frequencies are getting higher, the volume of the information extends in most of devices (for example, more storage is required for better quality of the photos in smartphones), and the existing memories (SRAM, DRAM, existing NVM) become insufficient for new challenges. MRAM is one of the emerging memories, which has promising parameters, that is why it is also important to take care of the reliability of this type of

memory. Built-in Self-Test (BIST) is an effective solution that is usually used to test embedded memories and can be adopted for MRAM as well. MRAM has the perspective to be a universal memory , as it is non-volatile and has a speed close to SRAM and a density close to DRAM at the same time.

2. Preliminaries

2.1. MRAM Structure

MRAM cell consists of a transistor and a device called a magnetic tunnel junction (MTJ). It consists of two ferromagnetic layers separated by an insulator (Figures 1,2,3). MTJ is a based on tunnel magnetoresistance (TMR) which occurs in MTJ and is quantum mechanical phenomenon. Electrons can tunnel from one layer to another because the insulator layer is very thin. One of the layers has a fixed direction of spins. The direction of spins of the second layer can be changed by applying voltage between two layers. MTJ can be represented as a variable resistance, which can be changed depending on the direction of spins in ferromagnetic layers. There are parallel and antiparallel cases. When magnetic spins are parallel, the resistance of the MTJ becomes lower, which corresponds to level "0". Accordingly, for a logical level "1", the MTJ is in an antiparallel state with high resistance.

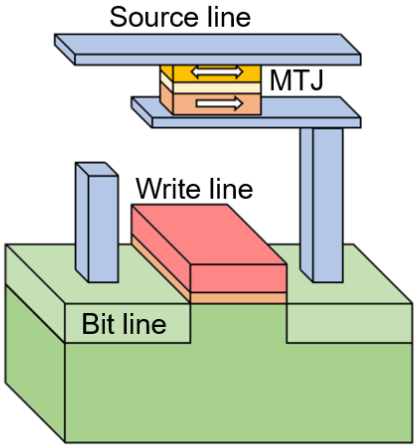

Fig. 1. MRAM bit cell.

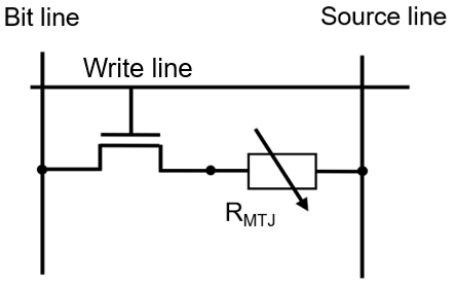

Fig. 2. MRAM bit cell schematic.

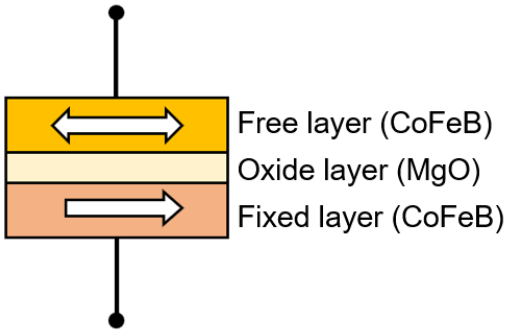

Fig. 3. MTJ schematic.

2.2. Faults specific to MRAM

Since MRAM has a different manufacturing technology in contrast to CMOS, it is required to explore defects, which can occur during manufacturing (resistive faults are shown in Figure 4). There are also other faults, which are not described because of MTJ nature. The main reason is the clear tunneling phenomenon, which has a certain probability. For example, the insulation layer thickness can change the MTJ resistance which can cause read failure. Some of MRAM specific faults are described in Table 1.

Table 1: Faults specific to MRAM

Stuck at P	MTJ is stuck at the parallel state (low resistance for MTJ).
Stuck at AP	MTJ is stuck at the antiparallel state (high resistance for MTJ).
Open	Weak connections between metals or other layers can cause open defects and correspondingly open fault because of high resistance.
Short	Short between ferromagnetic layers can occur during some manufacturing stages.
Transition fault	It is not possible to write 0 when a bit cell caries 1, and vice versa (it is assumed that initially memory has x value).
Coupling fault	Switching of the current bit cell causes flipping of the neighbor bit cell.
Incorrect read fault	Incorrect value after read operation (it means that the bit cell carries 0/1 but the read data is 1/0).

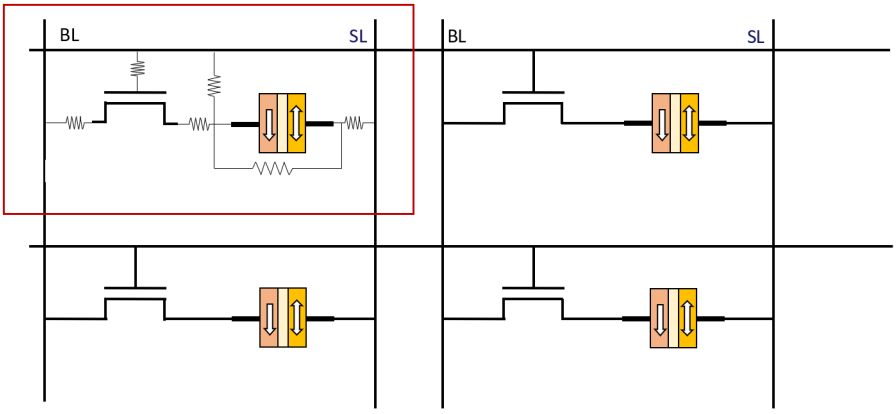

Fig. 4. Resistive faults for one bit cell (in red area).

2.3. Algorithms for Testing MRAM

Several algorithms for MRAM testing are suggested in [4]-[6]. [4] also offers an automated flow for defect injection and fault modeling, which is very useful for writing new test vectors for certain faults. [5] suggests a test algorithm, which covers most of the resistive defects described in the same paper. The proposed BIST architecture provides all the necessary operations to detect the above-mentioned defects.

3. MRAM BIST

There are different architectures of testing systems for different types of memories. During design implementation, it is important to take into account the hierarchical structure of the design, which contains memories, their sharing mechanism, test efficiency for that system, etc. Sometimes these and other factors make testing systems insufficient for executing certain types of algorithm or do not meet the given specification. The suggested testing system takes into account the above mentioned and other design specific difficulties. MRAM testing system consists of two main components: MRAM Processor and MRAM Memory Controller (Figure 5).

3.1. MRAM Memory Controller Components

Memory controller provides transmission of test data and control signals from processor directly to the memory, as well as the memory output-related analyses in backward direction. Controller has the following blocks as described in Table 2.

3.2. MRAM Processor Components

MRAM Processor Unit regulates connections and signals between memory controllers. It is responsible for address, data (pattern), redundancy generation, and executing instructions.

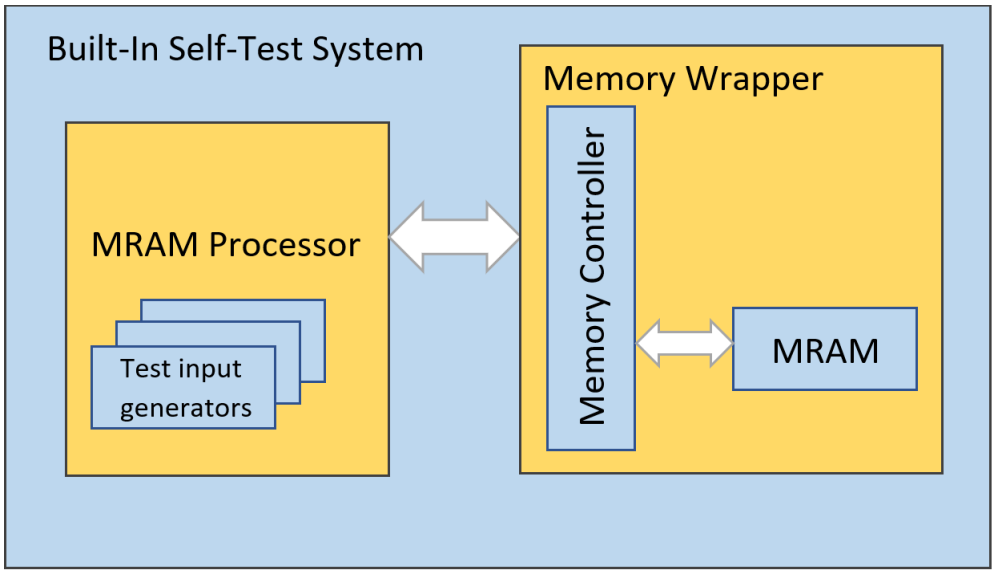

Fig. 5. Built-in Self-Test System.

Table 2: Memory controller's main components

Comparator	Compares output data with the expected ones. Sends theresult of comparison to the processor.
Redundancy Allocator	Makes repair signature according to error data.

It has a programmable buffer, which carries a march algorithm. Short introduction of some processor blocks are described below in Table 3.

Table 3: BIST Processors main components

Address Generator	Responsible for test address signal for the memories in wrappers. Different addressing modes are available.
Data Generator	Responsible for test input data for the memories in wrappers. Solid, checkerboard and other patterns are available.
Redundancy Generator	Collects repair data information from wrappers to perform memory repair.
BIST Controller	Controls march algorithm execution on memories (Figure 6).
Trim Controller	Executes search algorithms to find reference values for MRAM memories for efficient testing.

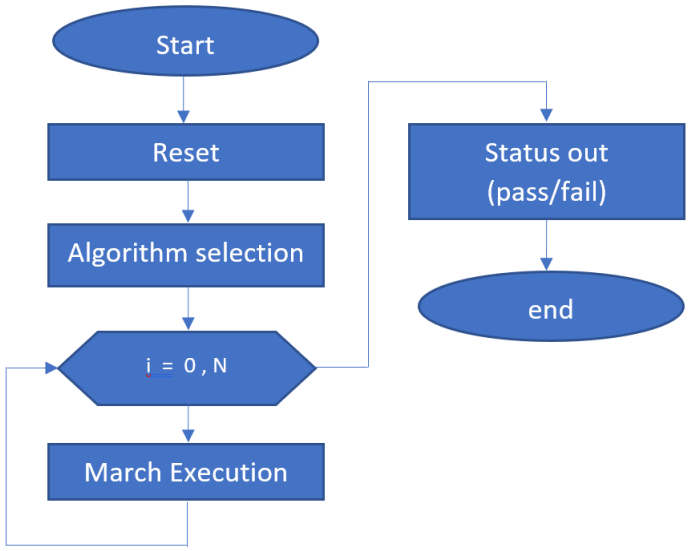

Fig. 6. Block Diagram for BIST flow.

4. Conclusion

Magnetic memory becomes more widespread nowadays thanks to its good characteristics and is considered to be the next universal memory. Therefore, it is highly important to well understand the faults inherent to this technology and develop a test solution addressing these types of faults. In this work, fault universe for MRAM memories is investigated and a specifically adjusted BIST architecture is proposed, which allows us to detect all these types of faults. Among other features, the proposed BIST solution has an algorithm programmable capability, which is used to code test algorithms for detecting specific fault types and an efficient test trimming mechanism used for searching MRAM reference bits.

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Ներդրված թեստավորման ճարտարապետություն մագնիսական հիշողությունների համար

Արմեն Վ. Բաբայան

Հայաստանի ազգային պոլիտեխնիկական համալսարան
e-mail: Armen.Babayan@synopsys.com

Ամփոփում

Մագնիսական կամայական ընտրությամբ հիշողությունը (MRAM) նոր ժամանակակից տեխնոլոգիաներից մեկն է, որն իր լավ պարամետրերի շնորհիվ կարող է դիտարկվել որպես հաջորդ համապիտանի հիշողություն: Այնուամենայնիվ, այս տիպի հիշողությունը պաշտպանված չէ անսարքություններից, և շատ կարևոր է հասկանալ այդ անսարքությունների դասակարգումը և մշակել թեստավորման համակարգ, որը դուրս կբերի դրանց հետևանքով առաջացող սխալները: Այս հոդվածում ներկայացված է ներդրված թեստավորման համակարգ (BIST) մագնիսական հիշողությունների համար, որը արդյունավետ կերպով հայտնաբերում է այդ տիպի հիշողություններին հատուկ անսարքությունները:

Բանալի բառեր՝ հիշողությունների ներդրված թեստավորում, հիշողությունների թեստավորում, մագնիսական հիշողություն, նորագույն հիշող սարք, համակարգ բյուրեղի վրա:

Архитектура встроенного самотестирования для магнитных памятей

Армен В. Бабаян

Национальнуй политехнический университет Армении
e-mail: Armen.Babayan@synopsys.com

Аннотация

Магнитная память с произвольным доступом (MRAM) - одна из новых современных технологий, которая благодаря своим хорошим параметрам может считаться следующей универсальной памятью.Тем не менее, этот тип памяти не гарантирован от дефектов, и очень важно понимать типологию неисправностей и разработать тестовое решение, которое устраняет ошибки вызванные неисправностями. В этой статье представлено решение встроенного самотестирования (BIST), которое, в частности, адаптировано для MRAM и эффективно устраняет его специфические неисправности.

Ключевые слова: самотестирование встроенной памяти, тестирование памяти, магнитная память, новейшая память, система на кристалле.