

Linear Cryptanalysis of SAFER-256

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Abstract

In this paper linear cryptanalysis of 256-bit block cipher SAFER-256 is presented. SAFER-256 is secure against differential cryptanalysis after 5 rounds.

Keywords: Linear cryptanalysis.

1. Introduction

In paper [1] the detailed construction and security analysis against differential analysis of block cipher SAFER-256 is introduced. In this paper the result of linear cryptanalysis [2] of SAFER-256 is presented. We follow the terminology and notation in [2].

The round function is applied to 256 bit plaintext $X = X_1X_2 \dots X_{32}$ with 6 times. The round function consists of the following four layers:

1. XOR/ADD, the first round key is "added" to the round input. Bytes 1,2,3,4,9,10,11,12,17,18,19,20,25,26,27,28 are added together bit-by-bit modulo 2 (XOR) bytes 5,6,7,8,13,14,15,16,21,22,23,24,29,30,31,32 are added together modulo 256 (ADD): $U = \text{XOR/ADD}(X, K_{2i-1})$.
2. Non-Linear (NL), where the values of bytes 1,2,3,4,9,10,11,12,17,18,19,20,25,26,27,28 are converted to $45^x \text{ modulo } 257$ (with the convention that 45^{128} is represented as 0) and the values of bytes 5,6,7,8,13,14,15,16,21,22,23,24,29,30,31,32 are converted to $\log_{45}x$ (with the convention that the output $\log_{45}0$ is represented by 128): $V = \text{NL}(U)$.
3. ADD/XOR, by this layer the second round key is inserted. The round key bytes 1,2,3,4,9,10,11,12,17,18,19,20,25,26,27,28 are added to the corresponding output bytes of linear layer modulo 256 (ADD) while the round key bytes 5,6,7,8,13, 14,15,16,21, 22,23,24, 29,30,31,32 are added to the corresponding output bytes of linear layer modulo 2 (XOR): $W = \text{ADD/XOR}(V, K_{2i})$.
4. Invertible Linear Transform or Pseudo-Hadamard Transform (PHT) consisting of four times applied *Armenian shuffle* and four times applied eight 2-PHT boxes: $Y = \text{PHT}(W)$, is equivalent to $Y = WM$, where M is called an invertible linear transformation matrix of SAFER-256 introduced in Fig 1.

2. Linear Cryptanalysis of SAFER-256

We will find effective homomorphic I/O sums to a cascade of half-rounds of SAFER-256.

At first we find all binary-valued homomorphisms for ADD/XOR and for XOR/ADD. There are $2^8 - 1$ binary-valued homomorphisms for 8 bit XOR, namely the functions defined as $l_{a_2}(V_2) := a_2 \circ V_2$, where a_2 is a non-zero binary 8-tuple " \circ " operation denotes the modulo two "dot product". There is only one binary-valued homomorphism for modulo 256 addition, namely the function l_{a_1} where $a_1 = 0000\ 0001 = 01$ (hex notation of byte). Hence, there exist $2^{144} - 1$ balanced homomorphisms for ADD/XOR, namely the functions l_a defined as $l_a(V) = a \circ V$ where a lies in the set of 256-tuples.

$$\mathcal{A} = \{a: a \in \{0,1\}^{256} \setminus \{00\}; a_1, a_2, a_3, a_4, a_9, a_{10}, a_{11}, a_{12}, a_{17}, a_{18}, a_{19}, a_{20}, a_{25}, a_{26}, a_{27}, a_{28}\} \in \{00, 01\}\}.$$

Similarly, there are $2^{144} - 1$ balanced homomorphism for XOR/ADD, namely the functions $l_b(V) = b * V$, where b lies in the set

$$\mathcal{B} = \{b: b \in \{0,1\}^{256} \setminus \{00\}; b_5, b_6, b_7, b_8, b_{13}, b_{14}, b_{15}, b_{16}, b_{21}, b_{22}, b_{23}, b_{24}, b_{29}, b_{30}, b_{31}, b_{32}\} \in \{00, 01\}\}.$$

The set of all homomorphic functions for XOR/ADD and the set of all homomorphic functions for ADD/XOR are subsets of the set of all linear binary-valued functions.

At first we consider the part of round (half-round) containing the PHT function. The following lemma specifies all homomorphic I/O sums that have non-zero imbalance. The input function must be balanced and homomorphic for ADD/XOR; the output function must be balanced and homomorphic for XOR/ADD. There are $(2^{144} - 1)^2$ such I/O sums, namely

$$S_{a,b}^{\text{PHT-hr}} := l_a(V) \oplus l_b(Y) \quad a \in \mathcal{A}, b \in \mathcal{B}.$$

Lemma 1: *For the PHT-half-round, the only homomorphic I/O sums that have non-zero imbalance are the $2^{32} - 1$ guaranteed I/O sums obtained by XOR-ing together any positive number of the 32 guaranteed I/O sums listed in Table 1.*

Since $I(S_{a,b}^{\text{PHT-hr}} | k_{2i}) = I(S_{a,b}^{\text{PHT}})$ for any $k_{2i} \in \{0,1\}^{256}$, where $S_{a,b}^{\text{PHT}} := l_a(W) \oplus l_b(Y)$, ($a \in \mathcal{A}$ and $b \in \mathcal{B}$) is an I/O sum for the PHT function alone, we will look for I/O sums $S_{a,b}^{\text{PHT}}$ with non-zero imbalance instead of looking for $S_{a,b}^{\text{PHT-hr}}$ with non-zero imbalance. So, our main purpose is to find $a \in \mathcal{A}$ and $b \in \mathcal{B}$ such that $S_{a,b}^{\text{PHT}}$ sum has the form $W_\alpha \oplus \phi(W_{256}, \dots, W_{\alpha+1}, W_{\alpha-1}, \dots, W_0)$ for some input bit W_α , since this implies that the I/O sum imbalance is 0.

First we consider PHT function. Table 2 shows three kind of dependences for some input and output bits. By using Table 2 we can iteratively show that I/O sums $S_{a,b}^{\text{PHT}}$ with none-zero imbalance cannot contain any of the output bits Y_{ij} , where $i = 1,2,3,4,9,10,11,12,17,18,19,20,25,26,27,28$ and $j = 1,2,3,4,5,6,7$.

Finally, we consider the $2^{32} - 1$ balanced output functions obtained as linear combinations of the remaining 32 output bits that might occur if $b \in \mathcal{B}$. For each of these output functions, we found all input functions such that $S_{a,b}^{\text{PHT}}$ doesn't depend linearly on any input bit. It is easy to show that $((a,b); a,b \in \{0,1\}^{256}, I(S_{a,b}^{\text{PHT}}) = 1)$ is a subgroup of $(\mathcal{A} \times \mathcal{B}, \oplus_{256\text{bits}})$. (In fact if $I(S_{a,b}^{\text{PHT}}) = 1$ and $I(S_{a',b'}^{\text{PHT}}) = 1$ for some 256 tuples a' and b' , then $I(S_{a \oplus a', b \oplus b'}^{\text{PHT}}) = I(S_{a,b}^{\text{PHT}} \oplus S_{a',b'}^{\text{PHT}}) = I(S_{a,b}^{\text{PHT}}) \cdot I(S_{a',b'}^{\text{PHT}}) = 1$ as well, which shows that $\mathcal{A} \times \mathcal{B}$ is closed under " \oplus ".) Thus, we obtain all I/O sums with non-zero imbalance, as is done in the statement of the lemma.

Table 1. Effective I/O sums for the PHT-function.

(a, b)	$l_b(Y)$	$l_a(W)$	$I(S_{a,b}^{PHT})$
(00000000000110011001000010010001, 10000000000000000000000000000000)	$Y1_0$	$W12_0 \oplus W13_0 \oplus W16_0 \oplus W17_0 \oplus W20_0 \oplus W25_0 \oplus W28_0 \oplus W32_0$	1
(00000000000110011111000011110101, 01000000000000000000000000000000)	$Y2_0$	$W12_0 \oplus W13_0 \oplus W16_0 \oplus W17_0 \oplus W18_0 \oplus W19_0 \oplus W20_0 \oplus W25_0 \oplus W26_0 \oplus W27_0 \oplus W28_0 \oplus W30_0 \oplus W32_0$	1
(10010001100100000001100100000000, 00100000000000000000000000000000)	$Y3_0$	$W1_0 \oplus W4_0 \oplus W8_0 \oplus W9_0 \oplus W12_0 \oplus W20_0 \oplus W21_0 \oplus W24_0$	1
(10010001100100000001111101000110, 00010000000000000000000000000000)	$Y4_0$	$W1_0 \oplus W4_0 \oplus W8_0 \oplus W9_0 \oplus W12_0 \oplus W20_0 \oplus W21_0 \oplus W22_0 \oplus W23_0 \oplus W24_0 \oplus W26_0 \oplus W30_0 \oplus W31_0$	1
(00011001000000001001000110010000, 00001000000000000000000000000000)	$Y5_0$	$W4_0 \oplus W5_0 \oplus W8_0 \oplus W17_0 \oplus W20_0 \oplus W24_0 \oplus W25_0 \oplus W28_0$	1
(00011001000000001111010111110000, 00000100000000000000000000000000)	$Y6_0$	$W4_0 \oplus W5_0 \oplus W8_0 \oplus W17_0 \oplus W18_0 \oplus W19_0 \oplus W20_0 \oplus W22_0 \oplus W24_0 \oplus W25_0 \oplus W26_0 \oplus W27_0 \oplus W28_0$	1
(00000110010001100100011000000000, 00000010000000000000000000000000)	$Y7_0$	$W6_0 \oplus W7_0 \oplus W10_0 \oplus W14_0 \oplus W15_0 \oplus W18_0 \oplus W22_0 \oplus W23_0$	1
(00000110010001100100111100011001, 00000001000000000000000000000000)	$Y8_0$	$W6_0 \oplus W7_0 \oplus W10_0 \oplus W14_0 \oplus W15_0 \oplus W18_0 \oplus W21_0 \oplus W22_0 \oplus W23_0 \oplus W24_0 \oplus W28_0 \oplus W29_0 \oplus W32_0$	1
(01100000011001000110010000000000, 00000000100000000000000000000000)	$Y9_0$	$W2_0 \oplus W3_0 \oplus W10_0 \oplus W11_0 \oplus W14_0 \oplus W18_0 \oplus W19_0 \oplus W22_0$	1
(01111001011011010110010000000000, 00000000010000000000000000000000)	$Y10_0$	$W2_0 \oplus W3_0 \oplus W4_0 \oplus W5_0 \oplus W8_0 \oplus W10_0 \oplus W11_0 \oplus W13_0 \oplus W14_0 \oplus W16_0 \oplus W18_0 \oplus W19_0 \oplus W22_0$	1
(100100001001000100000000000011001, 00000000001000000000000000000000)	$Y11_0$	$W1_0 \oplus W4_0 \oplus W9_0 \oplus W12_0 \oplus W16_0 \oplus W28_0 \oplus W29_0 \oplus W32_0$	1
(10010000100100010100011000011111, 00000000000100000000000000000000)	$Y12_0$	$W1_0 \oplus W4_0 \oplus W9_0 \oplus W12_0 \oplus W16_0 \oplus W18_0 \oplus W22_0 \oplus W23_0 \oplus W28_0 \oplus W29_0 \oplus W30_0 \oplus W31_0 \oplus W32_0$	1
(10010001000000000001100100001001, 00000000000010000000000000000000)	$Y13_0$	$W1_0 \oplus W4_0 \oplus W8_0 \oplus W20_0 \oplus W21_0 \oplus W24_0 \oplus W29_0 \oplus W32_0$	1
(11010111000001100001100100001001, 00000000000001000000000000000000)	$Y14_0$	$W1_0 \oplus W2_0 \oplus W4_0 \oplus W6_0 \oplus W7_0 \oplus W8_0 \oplus W14_0 \oplus W15_0 \oplus W20_0 \oplus W21_0 \oplus W24_0 \oplus W29_0 \oplus W32_0$	1
(00001001000110010000000010010001, 00000000000000010000000000000000)	$Y15_0$	$W5_0 \oplus W8_0 \oplus W12_0 \oplus W13_0 \oplus W16_0 \oplus W25_0 \oplus W28_0 \oplus W32_0$	1
(01101101011110010000000010010001, 00000000000000001000000000000000)	$Y16_0$	$W2_0 \oplus W3_0 \oplus W5_0 \oplus W6_0 \oplus W8_0 \oplus W10_0 \oplus W11_0 \oplus W12_0 \oplus W13_0 \oplus W16_0 \oplus W25_0 \oplus W28_0 \oplus W32_0$	1
(0110010001100000000000000001100100, 00000000000000000100000000000000)	$Y17_0$	$W2_0 \oplus W3_0 \oplus W6_0 \oplus W10_0 \oplus W11_0 \oplus W26_0 \oplus W27_0 \oplus W30_0$	1
(01101101011110010000000001100100, 00000000000000000100000000000000)	$Y18_0$	$W2_0 \oplus W3_0 \oplus W5_0 \oplus W6_0 \oplus W8_0 \oplus W10_0 \oplus W11_0 \oplus W12_0 \oplus W13_0 \oplus W16_0 \oplus W26_0 \oplus W27_0 \oplus W30_0$	1
(01000110000001100000000001000110, 00000000000000000001000000000000)	$Y19_0$	$W2_0 \oplus W6_0 \oplus W7_0 \oplus W14_0 \oplus W15_0 \oplus W26_0 \oplus W30_0 \oplus W31_0$	1
(01000110000001100001100101001111, 00000000000000000001000000000000)	$Y20_0$	$W2_0 \oplus W6_0 \oplus W7_0 \oplus W14_0 \oplus W15_0 \oplus W20_0 \oplus W21_0 \oplus W24_0 \oplus W26_0 \oplus W29_0 \oplus W30_0 \oplus W31_0 \oplus W32_0$	1
(00000000010001100100011000000110, 00000000000000000000010000000000)	$Y21_0$	$W10_0 \oplus W14_0 \oplus W15_0 \oplus W18_0 \oplus W22_0 \oplus W23_0 \oplus W30_0 \oplus W31_0$	1
(10010000110101110100011000000110, 00000000000000000000010000000000)	$Y22_0$	$W1_0 \oplus W4_0 \oplus W9_0 \oplus W10_0 \oplus W12_0 \oplus W14_0 \oplus W15_0 \oplus W16_0 \oplus W18_0 \oplus W22_0 \oplus W23_0 \oplus W30_0 \oplus W31_0$	1
(00011001000010011001000100000000, 00000000000000000000000100000000)	$Y23_0$	$W4_0 \oplus W5_0 \oplus W8_0 \oplus W13_0 \oplus W16_0 \oplus W17_0 \oplus W20_0 \oplus W24_0$	1
(01111001011011011001000100000000, 00000000000000000000000010000000)	$Y24_0$	$W2_0 \oplus W3_0 \oplus W4_0 \oplus W5_0 \oplus W8_0 \oplus W10_0 \oplus W11_0 \oplus W13_0 \oplus W14_0 \oplus W16_0 \oplus W17_0 \oplus W20_0 \oplus W24_0$	1
(0110010000000000000110000001100100, 00000000000000000000000010000000)	$Y25_0$	$W2_0 \oplus W3_0 \oplus W6_0 \oplus W18_0 \oplus W19_0 \oplus W26_0 \oplus W27_0 \oplus W30_0$	1
(011001000000000001111000011110101, 00000000000000000000000001000000)	$Y26_0$	$W2_0 \oplus W3_0 \oplus W6_0 \oplus W17_0 \oplus W18_0 \oplus W19_0 \oplus W20_0 \oplus W25_0 \oplus W26_0 \oplus W27_0 \oplus W28_0 \oplus W30_0 \oplus W32_0$	1
(0100011000000000000000011001000110, 00000000000000000000000001000000)	$Y27_0$	$W2_0 \oplus W6_0 \oplus W7_0 \oplus W22_0 \oplus W23_0 \oplus W26_0 \oplus W30_0 \oplus W31_0$	1
(11010111100100000000011001000110, 000000000000000000000000000010000)	$Y28_0$	$W1_0 \oplus W2_0 \oplus W4_0 \oplus W6_0 \oplus W7_0 \oplus W8_0 \oplus W9_0 \oplus W12_0 \oplus W22_0 \oplus W23_0 \oplus W26_0 \oplus W30_0 \oplus W31_0$	1
(00000000011001000110010001100000, 00000000000000000000000000001000)	$Y29_0$	$W10_0 \oplus W11_0 \oplus W14_0 \oplus W18_0 \oplus W19_0 \oplus W22_0 \oplus W26_0 \oplus W27_0$	1
(00000000011001001111010111110000, 00000000000000000000000000000100)	$Y30_0$	$W10_0 \oplus W11_0 \oplus W14_0 \oplus W17_0 \oplus W18_0 \oplus W19_0 \oplus W20_0 \oplus W22_0 \oplus W24_0 \oplus W25_0 \oplus W26_0 \oplus W27_0 \oplus W28_0$	1
(000000000100100010000100100011001, 00000000000000000000000000000010)	$Y31_0$	$W9_0 \oplus W12_0 \oplus W16_0 \oplus W21_0 \oplus W24_0 \oplus W28_0 \oplus W29_0 \oplus W32_0$	1
(00000110110101110000100100011001, 00000000000000000000000000000001)	$Y32_0$	$W6_0 \oplus W7_0 \oplus W9_0 \oplus W10_0 \oplus W12_0 \oplus W14_0 \oplus W15_0 \oplus W16_0 \oplus W21_0 \oplus W24_0 \oplus W28_0 \oplus W29_0 \oplus W32_0$	1

The half round containing the nonlinear function NL and find homomorphic I/O sums for NL that have non-zero imbalance. Here the input function is homomorphic for XOR/ADD and the output function is homomorphic for ADD/XOR. Such I/O sums can be obtained by summing I/O sums for its EXP and LOG blocks. For the function EXP with the input byte U1 and output byte V1, the only homomorphic I/O sums are

$$S_{a1,b1}^{EXP} = l_{a1}(U1) \oplus l_{b1}(V1), \text{ for } a1 \in B^8 \setminus \{00\}; b1 = 01.$$

The most effective ones are obtained when $(a1, b1)$ is equal to $(cd, 01)$ or $(ff, 01)$ (the imbalance being $\frac{28}{128}$) or to $(86, 01)$, $(bf, 01)$, $(c0, 01)$ or $(f7, 01)$ (the imbalance being $\frac{24}{128}$). Computing all these I/O sums for EXP, establishes the following.

Remark 1: $I(S_{01,01}^{EXP}) = I(S_{02,01}^{EXP}) = I(S_{03,01}^{EXP}) = 0$. Furthermore, for all $a1$ and $b1$ in B^8 , if $a1_7 = 0$, then $I(S_{a1,b1}^{EXP}) = 0$.

For the function LOG with the input U2 and output V2, the only homomorphic I/O sums are

$$S_{a2,b2}^{LOG} = l_{a2}(U2) \oplus l_{b2}(V2), \text{ for } a2 = 01; b2 \in B^8 \setminus \{00\}.$$

Their imbalance is easily deduced since $I(S_{a1,b1}^{EXP}) = I(S_{b1,a1}^{LOG})$.

Remark 2: For all $a1$ and $b1$ in B^8 , if $b1_7 = 0$, then $I(S_{a1,b1}^{LOG}) = 0$.

Finally we have link I/O sums for successive half rounds.

Theorem 1: The procedure for finding effective homomorphic I/O sums doesn't find an I/O sum with non-zero imbalance for cascade of half rounds taken in the same order as they are used in SAFER-256 and containing at least two PHT-layers.

Proof: Let $T_{a,b}^{PHT-hr}$, $T_{b,c}^{NL}$ and $T_{c,d}^{PHT-hr}$ be linked homomorphic half-round threefold sums with maximizing key function. If $T_{a,b}^{PHT-hr}$ and $T_{c,d}^{PHT-hr}$ have none zero imbalance, the 256 bit none zero masks a, b, c, d , can have a 1 only in the two least significant bits of each byte (bits of byte are numbered from 7 for the most significant bit to 0 for the least significant bit) (Lemma 1). Then $I(T_{b,c}^{NL}) = 0$ since the I/O sum average key imbalance is also 0 (Remark 1) Therefore, the sum of the three half-round threefold sums has imbalance 0.

One of the most effective I/O sums is $S_{a,b}^{NL-PHT-NL}$, where $a2, a10$ and $b13, b14, b31, b32$ are either cd or ff and other bytes of a and b are zero. Their imbalance is $\left(\frac{28}{128}\right)^6$, because

$$I(S_{ff,01}^{EXP}) = I(S_{cd,01}^{EXP}) = I(S_{01,ff}^{LOG}) = I(S_{01,cd}^{LOG}) = \frac{28}{128}$$

and because

$$I(S_{a,b}^{PHT}) = I(S_{a1 \oplus a2 \oplus a3 \oplus a4, b1 \oplus b2 \oplus b3 \oplus b4}^{PHT}) = I(S_{a1, b1}^{PHT}) \cdot I(S_{a2, b2}^{PHT}) = I(S_{a3, b3}^{PHT}) = I(S_{a4, b4}^{PHT}) = 1,$$

if

$$a1 \oplus a2 \oplus a3 \oplus a4 =$$

$$(01\ 00\ 00\ 01\ 00\ 00\ 00\ 01\ 00\ 00\ 00\ 00\ 00\ 00\ 00\ 00\ 00\ 00\ 00\ 01\ 01\ 00\ 00\ 01\ 00\ 00\ 00\ 00\ 01\ 00\ 00\ 01) \oplus$$

$$(01\ 01\ 00\ 01\ 00\ 01\ 01\ 00\ 00\ 00\ 00\ 00\ 01\ 01\ 00\ 00\ 00\ 00\ 01\ 01\ 00\ 00\ 01\ 00\ 00\ 00\ 00\ 01\ 00\ 00\ 01\ 00\ 00\ 00\ 00) \oplus$$

$$(00\ 00\ 00\ 00\ 00\ 00\ 00\ 00\ 01\ 00\ 00\ 01\ 00\ 00\ 00\ 01\ 00\ 00\ 00\ 00\ 01\ 00\ 00\ 01\ 00\ 00\ 00\ 01\ 00\ 00\ 00\ 01\ 00\ 00\ 00\ 01) \oplus$$

$$(00\ 00\ 00\ 00\ 00\ 00\ 01\ 01\ 00\ 01\ 01\ 00\ 01\ 00\ 01\ 01\ 01\ 00\ 00\ 00\ 00\ 01\ 00\ 00\ 01\ 00\ 00\ 01\ 00\ 00\ 01\ 00\ 00\ 00\ 01)$$

SAFER-256 համակարգի գծային վերլուծությունը

Ք. Կյուրեղյան

Անփոփում

Այս հոդվածում ներկայացված է 256 բիթ բլոկի երկարության SAFER-256 բլոկային ծածկագրական համակարգի գծային վերլուծությունը, որը դիֆերենցիալ վերլուծության նկատմամբ կայուն է 5 ռաունդից հետո:

Линейный криптоанализ алгоритма SAFER-256

К. Кюрегян

Аннотация

В данной статье представлен линейный криптоанализ блочного шифра SAFER-256, которая устойчива по отношению к дифференциальному анализу после 5 раундов.